TITLE OF THE INVENTION

METHOD OF ENCAPSULATING SEMICONDUCTOR DEVICES ON A PRINTED CIRCUIT BOARD, AND A PRINTED CIRCUIT BOARD FOR USE IN THE METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention generally relates to the manufacture of semiconductor devices. More particularly, the present invention relates to a method of encapsulating semiconductor chip packages attached to a printed circuit board, and to a printed circuit board used in the method.

2. Description of the Related Art

[0002] Electronic modules are generally formed by the mounting of several semiconductor chip packages to a printed circuit board, and recently, the trend has been to attach the chip packages to both sides of the printed circuit board to increase packing density.

[0003] The wafer level package (WLP) is one type of chip package mounted onto printed circuit boards. WLP's are characterized by external terminals that are distributed in a two-dimensional array over a surface of the semiconductor chip. This reduces the signal path of

the semiconductor chip to a package I/O location, thereby improving the operational speed of the device. Further, unlike other chip packages having peripheral leads extending from the sides of the package, the WLP occupies no more of the surface of the printed circuit board (PCB) than roughly the size of the chip itself.

[0004] The WLP typically contains metallic solder bumps which function as external terminals interconnecting the package to the printed circuit board. The solder bumps of the WLP device are attached to the printed circuit board and then encapsulated within an epoxy material to secure a reliable connection with the printed circuit board and to protect the WLP from an external environment. FIGS. 1 through 4 are cross-sectional views for explaining a conventional method of encapsulating WLP packages on opposite sides of a printed circuit board.

[0005] FIG. 1 shows a cross-sectional view of a typical wafer level package 14. The wafer level package generally includes a semiconductor chip 10 and a plurality of solder bumps 12 formed over a surface of the semiconductor chip 10. Though not shown, the solder bumps 12 are disposed in an array fashion on the surface of the semiconductor chip 10, and one or several rerouting

layers are interposed between the solder bump array and the semiconductor chip 10.

[0006] Referring to FIG. 2, wafer level packages 14 are attached to opposite sides of the a printed circuit board 18 as shown. In this manner, semiconductor chips 10 are electrically connected to the printed circuit board 18 through the solder bumps 12.

[0007] Referring to FIG. 3, the printed circuit board 18 is positioned in a mold body which generally includes an upper mold body portion 22 and a lower mold body portion (not shown). The upper mold body 22 has a mold cavity defined therein, and the upper mold body portion 22 is positioned on a side of the printed circuit board 18 so as to accommodate the wafer level package 14 attached on the upper side of the printed circuit board 18.

[0008] The upper mold body portion also has a mold inlet 24 which is defined adjacent the upper surface of the printed circuit board 18 and which is in fluid communication with the mold cavity. As represented by the arrow of FIG. 3, the mold cavity is filled with an encapsulating material 26 through this mold inlet 24. Preferably, the encapsulating material 26 is an epoxy molding compound (EMC).

[0009] Subsequently, though not shown, the resultant structure is turned upside down, and then the wafer level package on the other side of the printed circuit board is encapsulated in the same manner. FIG. 4 is a cross-sectional view of the completed electronic module, where the wafer level packages are encapsulated within the molded EMC on both sides of the printed circuit board 18.

[0010] As described above, in order to encapsulate the wafer level packages on both sides of the printed circuit board, it is necessary to execute the same molding process twice, i.e., once on each side of the printed circuit board. The inherent redundancy of the process has the net effect of increasing processing time and manufacturing costs.

SUMMARY OF THE INVENTION

[0011] According to on aspect of the present invention, a first semiconductor chip is attached to a first side of a printed circuit board, and a second semiconductor chip is attached to a second side of the printed circuit board opposite the first side of the printed circuit board. A mold is then used to form a first mold cavity which contains the first semiconductor chip over the first side of the printed circuit board, and to form a second mold cavity which contains the second semiconductor chip over

the second side of the printed circuit board. The first and second mold cavities are simultaneously filled with a fill material via a mold inlet, where the mold inlet is at least partially defined through an aperture in the printed circuit board from the first side to the second side.

[0012] According to another aspect of the present invention, a first semiconductor chip is attached to a first side of a non-disposable portion of printed circuit board, and a second semiconductor chip is attached to a second side of the non-disposable portion of the printed circuit board opposite the first side of the printed circuit board. A mold is used to form a first mold cavity which contains the first semiconductor chip over the first side of the printed circuit board, and to form a second mold cavity which contains the second semiconductor chip over the second side of the printed circuit board. The mold further forms a mold inlet which traverses a boundary between a disposable region and the non-disposable region of the printed circuit board. The first and second mold cavities are simultaneously filled with a fill material via the mold inlet. Then, the mold is removed to expose the fill material defined by the first and second cavities and further defined by the mold inlet. The disposable region of the printed circuit

board is then separated from the non-disposable region of the printed circuit board.

[0013] According to another aspect of the present invention, a semiconductor chip is attached to a first side of a non-disposable portion of printed circuit board. A mold is used to form a mold cavity which contains the semiconductor chip over the first side of the printed circuit board, where the mold further forms a mold inlet which traverses a boundary between a disposable region and the non-disposable region of the printed circuit board. The mold cavity is then filled with a fill material via the mold inlet, and the mold is removed to expose the fill material defined by the mold cavity and further defined by the mold inlet. The disposable region of the printed circuit board is then separated from the non-disposable region of the printed circuit board.

[0014] According to still another aspect of the present invention, a plurality of first semiconductor chips are attached to a first side of a printed circuit board, and a plurality of second semiconductor chips are attached to a second side of the printed circuit board opposite the first side of the printed circuit board. A mold is then used to form at least one first mold cavity which contains the first semiconductor chips over the first side of the printed circuit board, and to form at

least one second mold cavity which contains the second semiconductor chips over the second side of the printed circuit board. The first and second mold cavities are then simultaneously filled with a fill material via at least one mold inlet.

[0015] According to yet another aspect of the present invention, a plurality of first semiconductor chips are attached to a first side of a non-disposable portion of printed circuit board, and a plurality of second semiconductor chips are attached to a second side of the non-disposable portion of the printed circuit board opposite the first side of the printed circuit board. A mold is then used to form at least one first mold cavity which contains the first semiconductor chips over the first side of the printed circuit board, and to form at least one second mold cavity which contains the second semiconductor chips over the second side of the printed circuit board. The mold further forms at least one mold inlet which traverses a boundary between a disposable region and the non-disposable region of the printed circuit board. The first and second mold cavities are then simultaneously filled with a fill material via the mold inlet. The mold is then removed to expose the fill material defined by the first and second cavities and further defined by the mold inlet, and the disposable

region of the printed circuit board is separated from the non-disposable region of the printed circuit board.

[0016] According to still another aspect of the present invention, a plurality of semiconductor chips are attached to a first side of a non-disposable portion of printed circuit board. A mold is used to form at least one first mold cavity which contains the semiconductor chips over the first side of the printed circuit board, where the mold further forms at least one mold inlet which traverses a boundary between a disposable region and the non-disposable region of the printed circuit board. The at least one mold cavity is filled with a fill material via the mold inlet, and then the mold is removed to expose the fill material defined by the at least one mold cavity and further defined by the mold inlet, The disposable region of the printed circuit board is then separated from the non-disposable region of the printed circuit board.

[0017] According to another aspect of the present invention, an elongate printed circuit board is provided having an edge connector located on a first long edge thereof. A plurality of first wafer level packages are attached on a first surface of the printed circuit board and juxtaposed along the length of the printed circuit board between the first long edge and a second long edge

of the printed circuit board. A plurality of second wafer level packages are attached on a second surface of the printed circuit board opposite the first surface and aligned with the first wafer level packages, respectively. A mold is used to form at least one first mold cavity which contains the first wafer level packages over the first side of the printed circuit board, and to form at least one second mold cavity which contains the second wafer level packages over the second side of the printed circuit board. The first and second mold cavities then simultaneously filled with a fill material via at least one mold inlet which extends from the second edge of the printed circuit board to the first and second mold cavities.

[0018] According to still another aspect of the present invention, a printed circuit board includes a flat, elongate board body having a first surface and an opposite second surface, and further having a first long edge and an opposite second long edge. An edge connector is located on the first long edge of the board body. A first plurality of wafer level package mounting regions are located on the first surface of the board body and juxtaposed along the length of the board body between the first long edge and a second long edge, and a second plurality of wafer level package mounting regions are

located on the second surface of the board body and respectively aligned with the first plurality of wafer level package mounting regions. A plurality of mold inlet apertures extend through said board body and are respectively located between second long edge and the wafer level package mounting regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The various aspects and features of the present invention will become readily apparent from the detailed description that follows, with reference to the accompanying drawings, in which:

[0020] FIG. 1 is a cross-sectional schematic view of a conventional wafer level package (WLP);

[0021] FIGS. 2 through 4 are cross-sectional schematic views for explaining a conventional process for encapsulating wafer level packages on a printed circuit board;

[0022] FIG. 5 is a cross-sectional schematic view of a printed circuit board according to an embodiment of the present invention;

[0023] FIG. 6 is a top schematic view of a printed circuit board according to an embodiment of the present invention;

[0024] FIGS. 7 and 8 are cross-sectional schematic views for explaining a process for encapsulating wafer level packages on a printed circuit board according to another embodiment of the present invention;

[0025] FIG. 9 is a top schematic view of a printed circuit board according to another embodiment of the present invention;

[0026] FIG. 10 is a top schematic view of a printed circuit board according to another embodiment of the present invention;

[0027] FIGS. 11 through 13 are cross-sectional schematic views for explaining a process for encapsulating wafer level packages on a printed circuit board according to another embodiment of the present invention;

[0028] FIG. 14 is a top schematic view of a printed circuit board according to another embodiment of the present invention; and

[0029] FIG. 15 is a top schematic view of a printed circuit board according to another embodiment of the present invention.

DETAIL DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] The present invention will is described in detail below by way of several non-limiting preferred embodiments.

[0031] A printed circuit board (PCB) of an embodiment of the present invention will now be described with reference to the schematic illustrations of FIGS. 5 and 6, where FIG. 5 is a partial cross-sectional view of FIG. 6. As will be explained later, the PCB of this embodiment may be used to fabricate semiconductor devices in accordance with methods of manufacture of the present invention.

[0032] Referring to FIGS. 5 and 6, a generally flat and elongate board body 100 includes a first surface 150 and an opposite second surface 160, and a first long edge A and an opposite second long edge B. Preferably, the thickness, length and width dimensions of the board body 100 are in conformance with standards set by the Joint Electronic Device Engineering Council (JEDEC). The board body 100 is generally formed of multiple conductive patterned layers and insulating layers which are stacked on top of each other.

[0033] An edge connector 108 is located on the first long edge B of the board body 100. Device mounting regions 106 are located on the first surface 150 of the board body 100 and juxtaposed along the length of the

board body 100 between the first long edge A and the second long edge B. Each mounting region is preferably a conductive pad for the mounting of a wafer level package (WLP) device. Although not shown in FIGS. 5 and 6, device mounting regions are also located on the second surface 160 of the board body 100 and respectively aligned with the device mounting regions 106 on the first side 150 of the board body 100. In other words, the device attaching areas 106 on the first surface 150 are substantially a mirror image of those on the second surface 160.

[0034] A plurality of mold inlet apertures 104 extend through the board body 100 from the first side 150 to the second side 160. In this embodiment, the mold inlet apertures 104 are provided in one-to-one correspondence with each aligned pair device attaching areas 106. Also, in this embodiment, the mold inlet apertures 104 are located between second long edge A (opposite a connector 110, discussed later) and the respective wafer level package mounting regions 106, preferably in close proximity to the wafer level mounting regions 106.

[0035] An edge connector 108 is located on the first long edge B of the board body 100. Though not shown, the edge connector 108 is preferably configured as a comb of printed connector tabs. Electronic modules are typically

interconnected by mounting to a motherboard by means of a female edge connector physically affixed to and electrically connected with the motherboard. The edge connector 108 performs the dual functions of electrically connecting the module with the motherboard and physically supporting the module.

[0036] A process for encapsulating wafer level packages on a printed circuit board according to another embodiment of the present invention will now be described with reference to the cross-sectional schematic views of FIGS. 7 and 8.

[0037] Referring to FIGS. 7 and 8, first semiconductor chip 110A is attached to a first side of a printed circuit board 100, and a second semiconductor chip 110B is attached to an opposite second side of the printed circuit board 100. The printed circuit board 100 is equipped with a mold inlet aperture 122, and may be configured like the printed circuit board 100 discussed above in connection with FIGS. 5 and 6. In this case, the first and second semiconductor chips 110A, 110B are aligned with one another. Also, the first and second semiconductor chips 110A, 110B are preferably wafer level packages mounted on conductive pads of the printed circuit board 100.

[0038] After attaching the semiconductor chips 110A, 110B to the printed circuit board 100, the printed circuit board 100 is positioned in a mold body 121. The mold body 121 includes an upper mold body 121a and a lower mold body 121b. The upper mold body 121a has a first mold cavity 120a defined therein, and the lower mold body 121b has a second mold cavity 120b defined therein. The upper mold body 121a is positioned on a side of the printed circuit board 100 so as to accommodate the semiconductor chip 110B within the upper mold cavity 120a. Likewise, the lower mold body 121b is positioned on an opposite side of the printed circuit board 100 so as to accommodate the semiconductor chip 110A within the lower mold cavity 121b. At this time, the upper and lower mold cavities 120a, 120b are in fluid communication with the mold inlet aperture 122 of the printed circuit board 100.

[0039] The upper mold body 121a or the lower mold body 121b also has a mold inlet 123 which is defined adjacent a surface of the printed circuit board 18 and which is in fluid communication with the mold inlet aperture 122.

[0040] Next, the mold cavities 120a, 120b are simultaneously filled. That is, referring to the arrows and the region C of FIG. 8, an encapsulating material is fed into the mold inlet 123 so as to flow into the mold

cavities 120a, 120b. The mold cavity on the opposite side of the printed circuit board 100 to the mold inlet 123 is filled through the mold inlet aperture 122. As should be apparent from FIG. 8, the mold inlet aperture 122 of the printed circuit board 100 allows for the simultaneous filling of the mold cavities 120a and 120b.

[0041] Upon setting of the encapsulating material, the mold body 121 is removed. FIG. 7 is a cross-sectional view of the completed electronic module. In a preferred embodiment, wafer level packages 110A, 110B are encapsulated within molded EMC 120 on both sides of the printed circuit board 100.

[0042] In the description above, only first and second semiconductor chips 110A, 110B are shown and discussed. However, referring to FIG. 6, a preferred process is to mounted a plurality of semiconductor chips on the respective pads 106 of both sides of the printed circuit board. In this case, the upper mold body may define a plurality of upper mold cavities each in fluid communication with a respective one of the mold inlet apertures 104. Likewise, the lower mold body may define a plurality of lower mold cavities each in fluid communication with a respective one of the mold inlet apertures 104. The upper mold body and/or the lower mold body may then include one or more mold inlets in fluid

communication with the mold inlet apertures 104. In this manner, the plurality of upper mold cavities and the plurality of lower mold cavities can all be filled with encapsulating material as the same time.

[0043] In the embodiment of FIG. 6, the mold inlet apertures 104 are provided in one-to-one correspondence with the device mounting areas 106. However, the invention is not limited in this manner. For example, as shown in FIG. 9, two or more adjacent device mounting areas 106 may share the same mold inlet aperture 104.

[0044] FIG. 10 is a top schematic view of a printed circuit board according to another embodiment of the present invention. In this embodiment, a plurality of device mounting regions 106 are provided on at least one side of a board body 101, and an edge connector 108 is located at one edge B of the board body 101.

[0045] The board body 101 is divided into a disposable portion 130 and a non-disposable portion 140. As shown, the disposable portion is located along the edge A of the board body 101, opposite the connector 108. Preferably, the thickness, length and width dimensions of the non-disposable portion 140 of the board body 100 are in conformance with standards set by the Joint Electronic Device Engineering Council (JEDEC).

[0046] Finally, a plurality of mold inlet apertures 104 are located in the disposable portion 130. In this example, the mold inlet apertures are provided in one-to-one correspondence with the device mounting regions 106.

[0047] A process for encapsulating wafer level packages on a printed circuit board according to another embodiment of the present invention will now be described with reference to the cross-sectional schematic views of FIGS. 11 through 13.

[0048] Referring first to FIG. 11, first and second wafer level packages 110 are attached to opposite sides of a printed circuit board, and then encapsulated with an epoxy mold compound in the same manner as described above in connection with FIGS. 7 and 8. The printed circuit board may be configured in the same manner as that shown in FIG. 6.

[0049] Next, referring to FIG. 12, a saw blade or press apparatus is used to remove the disposable region 130 from the circuit board body 101. The resultant final module product is shown in FIG 13.

[0050] The embodiment of FIGS. 11 through 13 is advantageous in that portions of the printed circuit board of the final product are not occupied by the mold inlet apertures. That is, the high density and complexity in the conductive patterns of the printed

circuit board may make it difficult to find room for and design around the mold inlet apertures. This difficulty may be overcome by locating the mold inlet apertures in a disposable region of the board body, and then separating the disposable region to obtain the final product.

[0051] In the embodiment of FIG. 10, the mold inlet apertures 104 are provided in one-to-one correspondence with the device mounting areas 106. However, the invention is not limited in this manner. For example, as shown in FIG. 14, two or more adjacent device mounting areas 106 may share the same mold inlet aperture 104.

[0052] Likewise, in the embodiment of FIG. 10, all of the mold inlet apertures are located in the disposable region 130. However, the invention is not limited in this manner. For example, as shown in FIG. 15, some of the mold inlet apertures may be located in the non-disposable region 140, while others are located in the disposable region 130. This type of configuration may provide flexibility when optimizing the quality of the mold process.

[0053] In the drawings and specification, there have been disclosed typical preferred embodiments of this invention and, although specific examples are set forth, they are used in a generic and descriptive sense only and not for purposes of limitation. For example, in the

embodiments above, the mold cavities on opposite sides of the printed circuit board are simultaneously filled using an aperture in the printed circuit board. However, it is also possible to simultaneously fill the mold cavities by providing respective mold inlets extending from an edge of the printed circuit board on opposite sides of the printed circuit board. As another example, it is further possible to apply the embodiments in which the disposable portion of the printed circuit board is used to form part of the mold inlet to the case where a semiconductor chip is attached to one side only of the printed circuit board. It should therefore be understood the scope of the present invention is to be construed by the appended claims, and not by the exemplary embodiments.